

RoHS Compliant

SATA-Disk Chip II

Specification

August 18, 2009

Version 1.1

Features:

- **Standard Serial ATA 2.5 (Gen. 2)**
 - Serial ATA 2.5 (Gen. 2)
 - SATA II, 3.0 Gbps
 - ATA command set compatible
- **Connector type**
 - Standard 32/18 pin 600mil DIP
- **Low power consumption (typical)**
 - Supply voltage: 3.3V
 - Active mode: 300 mA
 - Idle mode: 197 mA
- **Performance**
 - Burst transfer rate: 300 MB/sec
 - Sustained read: 54 MB/sec
 - Sustained write: 54 MB/sec
- **Capacity**
 - 1, 2, 4, 8 GB
- **NAND Flash Type: SLC**
- **Temperature ranges**
 - Operation: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Intelligent endurance design**
 - Built-in hardware BCH ECC, correcting 8-bit or 15-bit error per 512-byte data sector
 - Static Wear-Leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
 - Flash Bad-Block Management
 - Power Failure Management
 - Quick Erase
 - S.M.A.R.T. technology
- **RoHS compliant**

Table of Contents

1. GENERAL DESCRIPTION	3
2. FUNCTIONAL BLOCK	4
2.1 FUNCTIONAL SPECIFICATIONS.....	4
2.1.1 ATA Mode Support	4
2.2.2 Performance	4
2.2 ENVIRONMENTAL SPECIFICATIONS	5
3. PIN ASSIGNMENTS	6
3.1 32 PINS (16 X 2).....	6
3.2 18 PINS (7X2 + 2X2).....	7
4. FLASH MANAGEMENT	8
4.1 ERROR CORRECTION/DETECTION	8
4.2 BAD BLOCK MANAGEMENT	8
4.3 WEAR LEVELING	8
4.4 POWER FAILURE MANAGEMENT	8
4.5 QUICK ERASE	8
4.6 S.M.A.R.T. TECHNOLOGY	9
5. SOFTWARE INTERFACE	10
5.1 COMMAND SET	10
6. PHYSICAL CHARACTERISTICS	12
6.1 DIMENSION OF 32 PINS (16X2).....	12
6.2 DIMENSION OF 18 PINS (7X2 + 2X2)	14
7. PRODUCT ORDERING INFORMATION	16
7.1 PRODUCT CODE DESIGNATIONS	16
7.2 VALID COMBINATIONS	17

1. General Description

Apacer's SATA-Disk Chip (SDC) is a high performance, embedded flash memory data storage system. This product is designed for embedded flash storage applications with expanded functionality and is a cost-effective replacement for a conventional IDE hard disk drive. SDCs have a built-in micro-controller and file management firmware that communicates with SATA standard interfaces; therefore, SDCs do not require additional or proprietary host software such as Flash File System (FFS) and Memory Technology Driver (MTD) software. Packaged in a 600 mil 32 or 18 round pin DIP package for easy and cost-effective mounting to a system motherboard, SDCs are designed to work at 3.3 Volts and use a standard SATA driver that is part of all major operating systems such as Microsoft's Windows series, Apple's MAC OS family, and UNIX variants.

In addition to buffer management through dynamical allocation, SDC adopts the static wear-leveling scheme to allow uniform use of all storage blocks, ensuring that the lifetime of a flash media can be significantly increased and the disk performance is optimized as well. SDC provides the S.M.A.R.T. feature complies to the SATA Rev.2.6, ATA/ATAPI-7 specifications and uses the standard SMART command B0h to read data from the drive. This feature protects the user from unscheduled downtime by monitoring and storing critical drive performance.

2. Functional Block

The SATA-Disk Chip (SDC) includes the SATA and Flash Management controllers, and flash media, as well as the SATA standard interface. Figure 2-1 shows the functional block diagram.

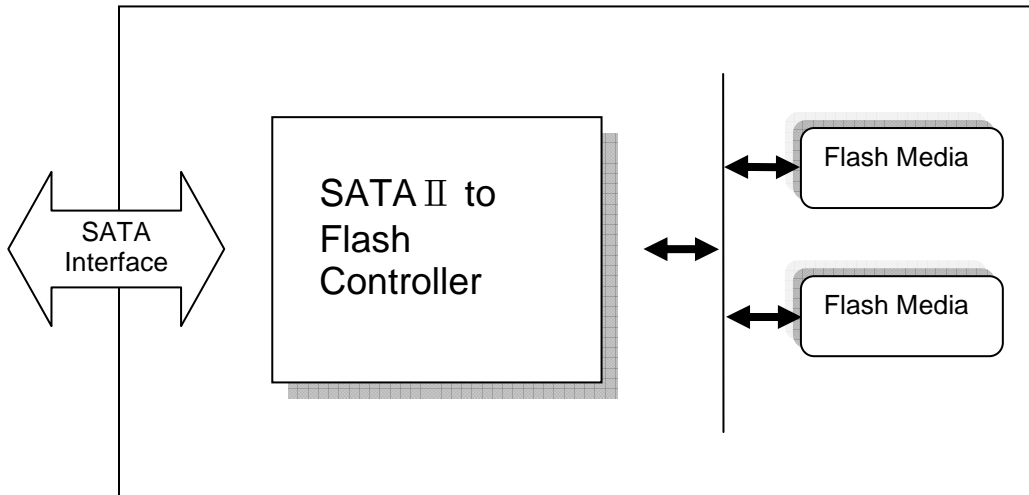


Figure 2-1: Functional block diagram

2.1 Functional Specifications

2.1.1 ATA Mode Support

The SATA-Disk Chip supports the following ATA operating modes:

- Supports up to PIO Mode-4
- Supports up to Multi-word DMA Mode-2
- Supports up to Ultra DMA Mode-5

2.2.2 Performance

Performance of SATA-Disk Chip is shown in table 2-1

Table 2-1: Performance specifications

Capacity	1 GB	2 GB	4 GB	8 GB
Performance				
Sustained read (MB/s)	27	37	45	54
Sustained write (MB/s)	14	12	45	54

2.2 Environmental Specifications

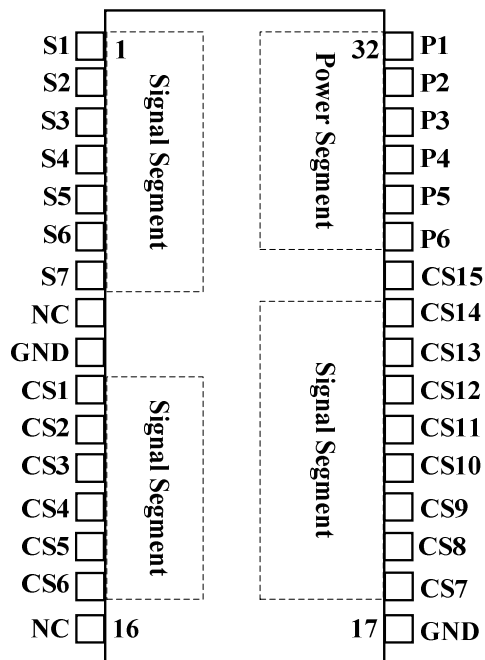
Environmental specification of the SATA-Disk Chip (SDC) product family which follows the MIL-STD-810F standards is available as shown in Table 2-2.

Table 2-2: Environmental specifications

Environment		Specification
Temperature	Operation	-40°C to 85°C
	Storage	-40°C to 100°C
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operation)		Sine wave: 20~2000Hz, 16.3g (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)

3. Pin Assignments

3.1 32 pins (16 x 2)

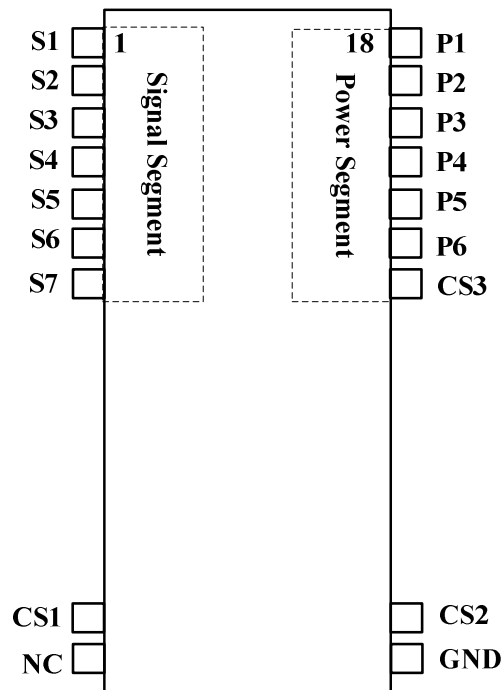


Pin	Name	Type ¹	Pin	Name	Type ¹
1	S1	GND	17	GND	GND
2	S2	RX+	18	CS7	Data Act.
3	S3	RX-	19	CS8	RS
4	S4	GND	20	CS9	RS
5	S5	TX-	21	CS10	RS
6	S6	TX+	22	CS11	RS
7	S7	GND	23	CS12	RS
8	NC	-	24	CS13	RS
9	GND	GND	25	CS14	RS
10	CS1	RS1	26	CS15	RS/WP
11	CS2	RS	27	P6	NA/UGND
12	CS3	RS	28	P5	NA/USB+
13	CS4	RS	29	P4	NA/USB-
14	CS5	RS	30	P3	NA/UVCC
15	CS6	PHY RDY	31	P2	GND
16	NC	-	32	P1	VCC3.3

1. RS: Reserved

SATA-Disk Chip II
AP-SDCxxxxXQANS-ETB

3.2 18 pins (7x2 + 2x2)



Pin	Name	Type ¹	Pin	Name	Type ¹
1	S1	GND	10	GND	GND
2	S2	RX+	11	CS2	Data Act.
3	S3	RX-	12	CS3	RS/WP
4	S4	GND	13	P6	NA/UGND
5	S5	TX-	14	P5	NA/USB+
6	S6	TX+	15	P4	NA/USB-
7	S7	GND	16	P3	NA/UVCC
8	CS1	PHY RDY	17	P2	GND
9	NC	-	18	P1	VCC3.3

4. Flash Management

4.1 Error Correction/Detection

SDC implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 8 bits or 15 bits error in 512 bytes.

4.2 Bad Block Management

Although bad blocks on the flash media are already identified by the flash manufacturer, they can also be accumulated over time during operation. SDC's controller maintains a table that lists those normal blocks with disk data, the free blocks for wear leveling, and bad blocks with errors. When a normal block is detected broken, it is replaced with a free block and listed as a bad block. When a free block is detected broken, it is then removed from the free block list and marked as a bad block.

During device operation, this ensures that newly accumulated bad blocks are transparent to the host. The device will stop file write service once there are only two free blocks left such that the read function is still available for copying the files from the disk into another.

4.3 Wear Leveling

The NAND flash devices are limited by a certain number of write cycles. When using a FAT-based file system, frequent FAT table updates are required. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole SSD, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. This scheme is called wear leveling.

Apacer's wear-leveling scheme is achieved both via buffer management and Apacer-specific static wear leveling. They both ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

4.4 Power Failure Management

The Low Power Detection on the controller initiates crucial data saving before the power supplied to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected power-off.

4.5 Quick Erase

Accomplished by the Secure Erase (SE) command, which added to the open ANSI standards that control disk drives, "Quick Erase" is built into the disk drive itself and thus far less susceptible to malicious software attacks than external software utilities. It is a positive easy-to-use data destroy command, amounting to electronic data shredding. Executing the command causes a drive to internally completely erase all possible user data. This command is carried out within disk drives, so no additional software is required. Once executed, neither data nor the erase counter on the device would be recoverable, which blurs the accuracy of device lifespan. The process to erase will not be stopped until finished while encountering power failure, and will be continued when power is back on.

4.6 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

Apacer's SDC uses the standard SMART command B0h to read data from the drive for SMART feature as the SATA Rev.2.6 ATA/ATAPI-7 specifications. Based on the SFF-8035i Rev. 2.0 specifications, Apacer SMART defines 3 vendor-specified SMART Attribute IDs (E5h, EAh-EBh, and E8h) in the SDC. They represent Flash ID, maximum erase count, average erase count, good block count, free-list block count, and firmware version information. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the SDC is in critical condition.

5. Software Interface

5.1 Command Set

This section defines the software requirements and the format of the commands the host sends to the SATA-Disk Chip (SDC). Commands are issued to the SDC by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 5-1: Command set (1 of 2)

Command	Code	FR ¹	SC ²	SN ³	CY ⁴	DH ⁵	LBA ⁶
Check-Power-Mode	E5H	-	-	-	-	D ⁸	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Flush-Cache	E7H	-	-	-	-	D	-
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H	-	Y	-	-	D	-
Idle-Immediate	E1H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	10H	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	-	Y	Y	-
Set-Features	EFH	Y ⁷	-	-	-	D	-

SATA-Disk Chip II

AP-SDCxxxxXQANS-ETB



Table 5-1: Command set (2 of 2)

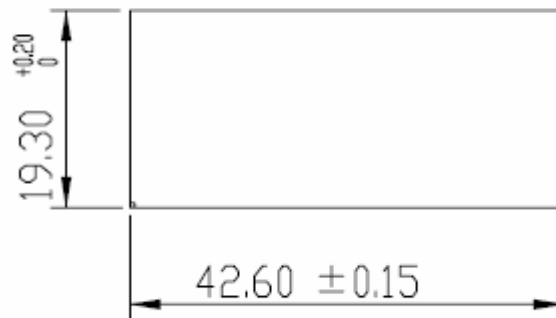
Command	Code	FR ¹	SC ²	SN ³	CY ⁴	DH ⁵	LBA ⁶
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Sleep	E6H	-	-	-	-	D	-
SMART	B0H	Y	Y	Y	Y	D	
Standby	E2H	-	-	-	-	D	-
Standby-Immediate	E0H	-	-	-	-	D	-
Write-DMA	CAH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H	-	Y	Y	Y	Y	Y

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command.
8. For the Drive/Head register:
 Y means both the SDC and Head parameters are used
 D means only the SDC parameter is valid and not the Head parameter

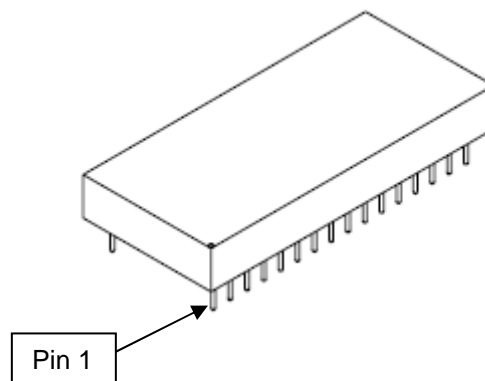
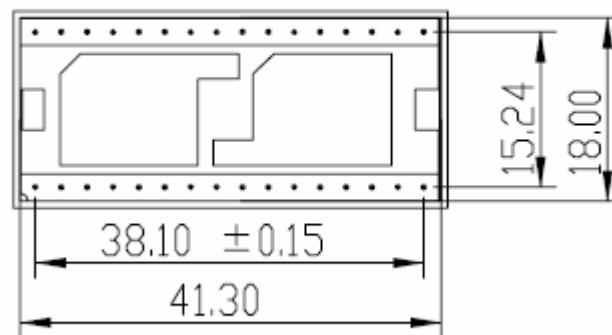
6. Physical Characteristics

6.1 Dimension of 32 pins (16x2)

TOP VIEW

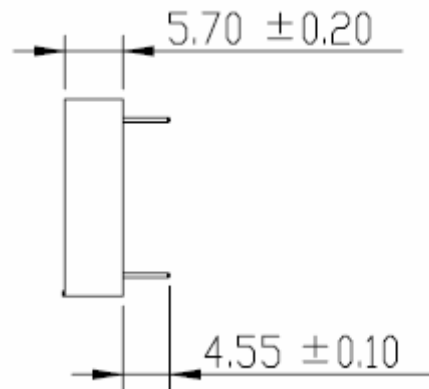
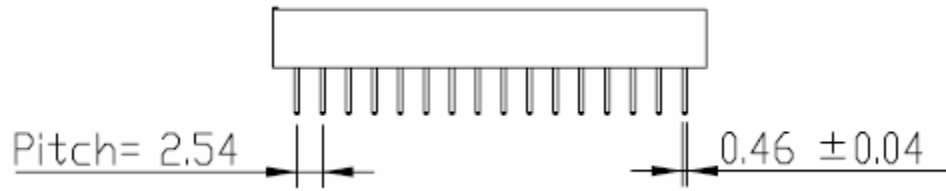


BOTTOM VIEW



Unit: mm
Tolerance: ± 0.25

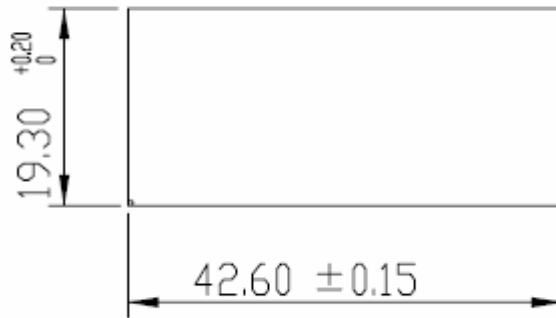
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AP-SDCxxxxXQANS-ETB



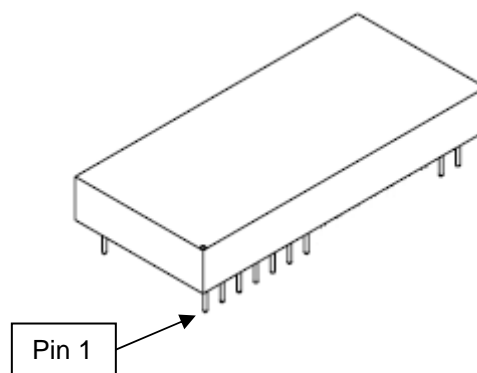
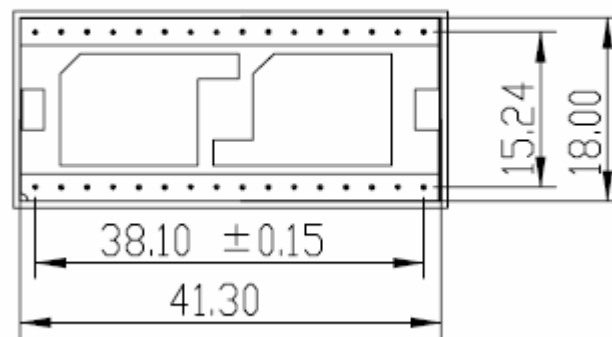
Unit: mm
Tolerance: ± 0.25

6.2 Dimension of 18 pins (7x2 + 2x2)

TOP VIEW

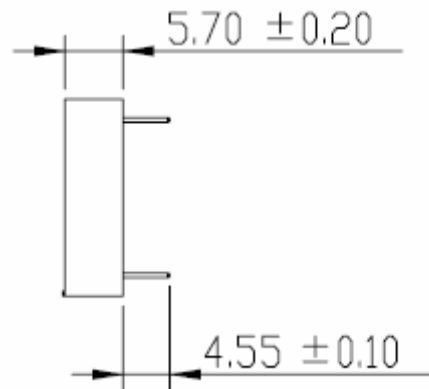
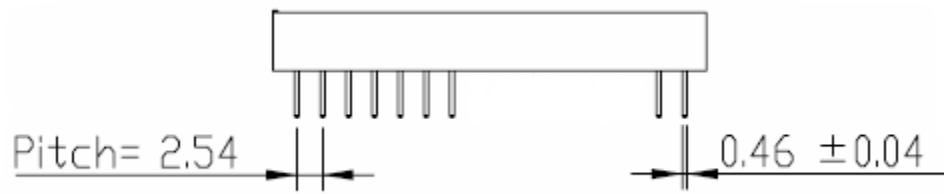


BOTTOM VIEW



Unit: mm
Tolerance: ± 0.25

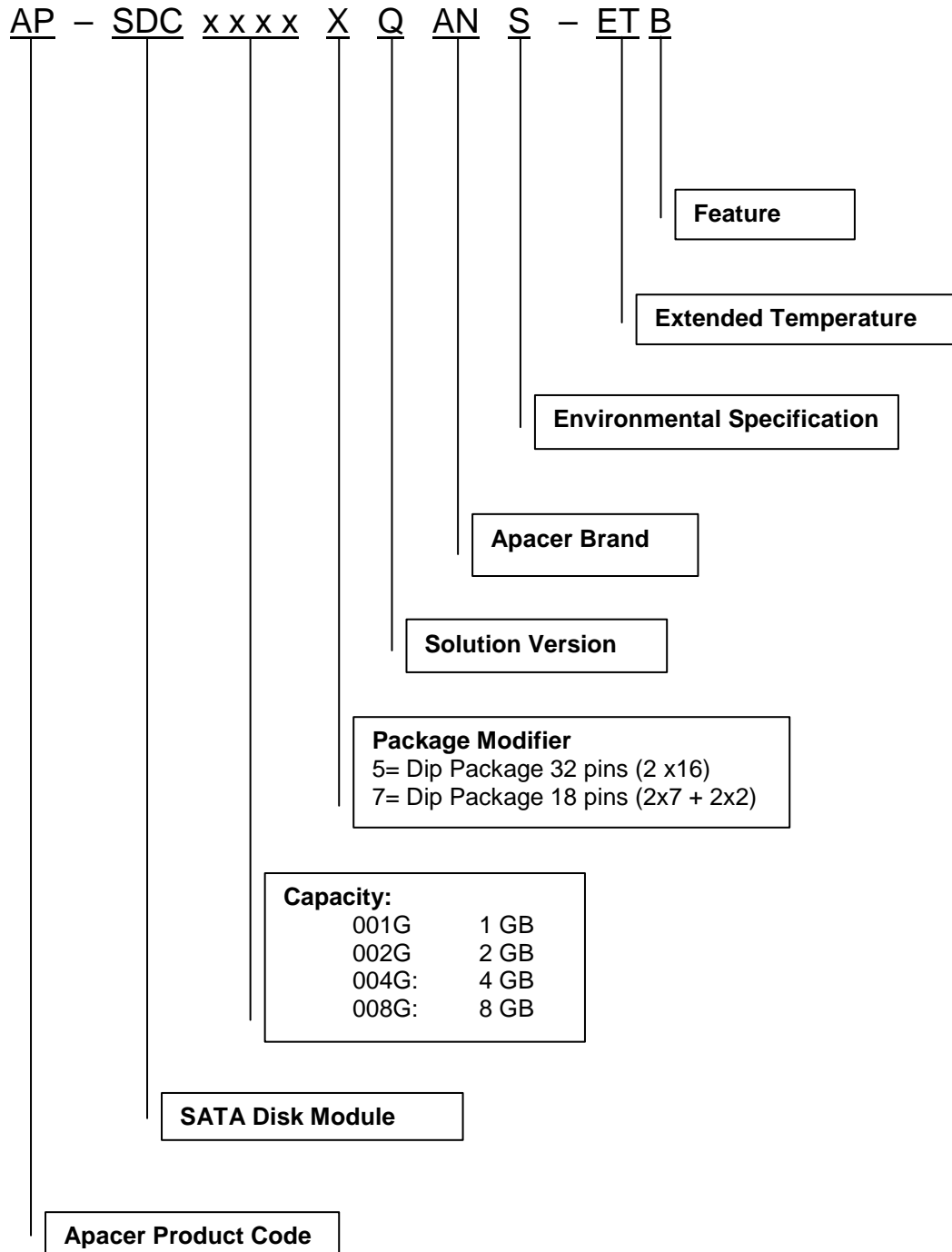
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AP-SDCxxxxXQANS-ETB



Unit: mm
Tolerance: ± 0.25

7. Product Ordering Information

7.1 Product Code Designations



7.2 Valid Combinations

SDCII 32 pin

Capacity	Model Number
1GB	AP-SDC001G5QANS-ETB
2GB	AP-SDC002G5QANS-ETB
4GB	AP-SDC004G5QANS-ETB
8GB	AP-SDC008G5QANS-ETB

SDCII 18 pin

Capacity	Model Number
1GB	AP-SDC001G7QANS-ETB
2GB	AP-SDC002G7QANS-ETB
4GB	AP-SDC004G7QANS-ETB
8GB	AP-SDC008G7QANS-ETB

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Date	Description	Remark
0.1	03/17/2009	Preliminary release	
0.2	03/30/2009	Updated product ordering information	
0.3	04/02/2009	Updated feature details & context wordings	
0.4	04/03/2009	Updated context details	
0.5	06/15/2009	Updated product ordering information	
1.0	08/04/2009	Official release	
1.1	08/18/2009	Updated performance	

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